16-BIT TO 8-BIT MULTIPLEXER/DEMULTIPLEXER GIGABIT ETHERNET LAN SWITCH WITH POWER DOWN MODE

Check for Samples: TS3L501E

FEATURES

- **Integrated Power Down Mode**
- **Wide Bandwidth (BW = 600 MHz Typ)**
- **Low Crosstalk (X_{TALK} = −37 dB Typ @ 250 MHz)**
- **Low Bit-to-Bit Skew ($t_{sk(o)}$ = 100 ps Max)**
- **Low and Flat ON-State Resistance (r_{on} = 4 Ω Typ, $r_{on(flat)}$ = 0.5 Ω Typ)**
- **Low Input/Output Capacitance (C_{ON} = 9 pF Typ)**
- **Rail-to-Rail Switching on Data I/O Ports (0 to 3.6 V)**
- **V_{CC} Operating Range From 3 V to 3.6 V**
- **Support Power Down Mode**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance (A, B, C, LED pins)**
    - **± 4-kV IEC61000-4-2, Contact Discharge**
    - **6-kV Human Body Model Per JESD22-A114E (Switch I/O pins to GND)**
- **ESD Performance (All pins)**
    - **2-kV Human Body Model Per JESD22-A114E**
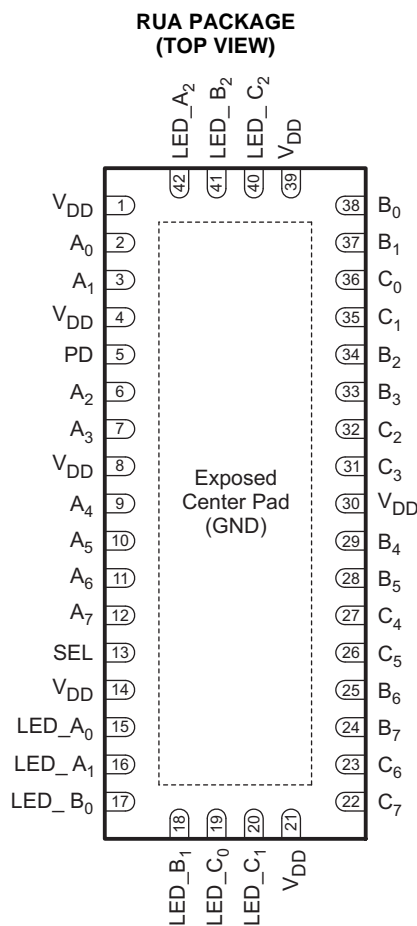
APPLICATIONS

- **10/100/1000 Base-T Signal Switching**
- **Differential (LVDS, LVPECL) Signal Switching**
- **Audio/Video Switching**
- **Hub and Router Signal Switching**

RUA PACKAGE
(TOP VIEW)

Pin	Name		Pin	Name
1	V_{DD}		38	B_0
2	A_0		37	B_1
3	A_1		36	C_0
4	V_{DD}		35	C_1
5	PD		34	B_2
6	A_2		33	B_3
7	A_3		32	C_2
8	V_{DD}		31	C_3
9	A_4		30	V_{DD}
10	A_5		29	B_4
11	A_6		28	B_5
12	A_7		27	C_4
13	SEL		26	C_5
14	V_{DD}		25	B_6
15	LED_A_0		24	B_7
16	LED_A_1		23	C_6
17	LED_B_0		22	C_7

Top pins: 42 LED_A_2, 41 LED_B_2, 40 LED_C_2, 39 V_{DD}

Bottom pins: 18 LED_B_1, 19 LED_C_0, 20 LED_C_1, 21 V_{DD}

Exposed Center Pad (GND)

The exposed center pad must be connected to GND.

DESCRIPTION/ORDERING INFORMATION

The TS3L501E is a 16-bit to 8-bit multiplexer/demultiplexer LAN switch with a single select (SEL) input and Power down Mode input. The device provides additional I/Os for switching status indicating LED signals and includes high ESD protection. SEL input controls the data path of the multiplexer/demultiplexer. Power down input can put the device into the standby mode for minimizing current consumption per mode selection.

The device provides a low and flat ON-state resistance (Ron) and an excellent ON-state resistance match. Low input/output capacitance, high bandwidth, low skew, and low crosstalk among channels make this device suitable for various LAN applications, such as 10/100/1000 Base-T. This device can be used to replace mechanical relays in LAN applications. It also can be used to route signals from a 10/100 Base-T Ethernet transceiver to the RJ-45 LAN connectors in laptops or in docking stations.

It is characterized for operation over the free-air temperature range of −40ºC to 85ºC.

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TS3L501E

Table 1. ORDERING INFORMATION

T_A	PACKAGE[1].[2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	TQFN − RUA	Tape and reel	TS3L501ERUAR	TK501E

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

LOGIC DIAGRAM (POSITIVE LOGIC)

Product Folder Link(s): TS3L501E
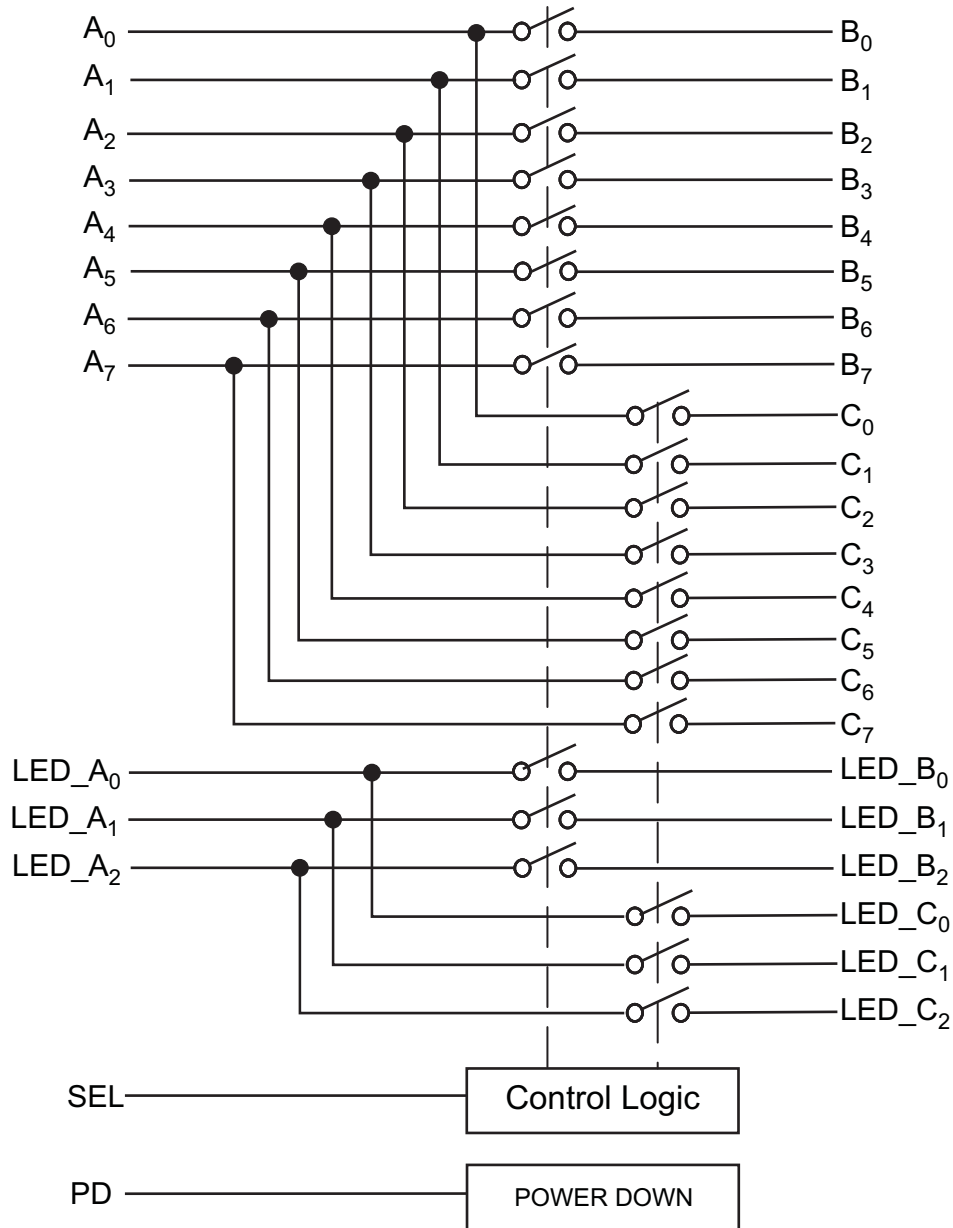
FUNCTION TABLE

PD	SEL	FUNCTION
L	L	A_n to B_n, LED_A_n to LED_B_n
L	H	A_n to C_n, LED_A_n to LED_C_n
H	X	Hi-Z

PIN DESCRIPTION

NAME	DESCRIPTION
A_n	Port A DeMux I/O
B_n, C_n	Port B, C Mux I/O
LED_A_n, LED_B_n, LED_C_n	LED Mux I/O
SEL	Select Input
PD	Power Down Input, Active High
GND	Ground
V_{DD}	Power

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage range		−0.5	4.6	V
V_{IN}	Control input voltage range[2] [3]		−0.5	7	V
$V_{I/O}$	Switch I/O voltage range[2] [3] [4]		−0.5	7	V
I_{IK}	Control input clamp current	$V_{IN} < 0$		−50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$		−50	mA
$I_{I/O}$	ON-state switch current[5]			±128	mA
	Continuous current through V_{DD} or GND			±100	mA
θ_{JA}	Package thermal impedance[6]			51.2	°C/W
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS[1]

		MIN	MAX	UNIT
V_{DD}	Supply voltage	3	3.6	V
V_{IH}	High-level control input voltage (SEL)	2	5.5	V
V_{IL}	Low-level control input voltage (SEL)	0	0.8	V
V_{IN}	Input voltage (SEL)	0	5.5	V
$V_{I/O}$	Input/output voltage	0	V_{DD}	V
T_A	Operating free-air temperature	−40	85	°C

(1) All unused control inputs of the device must be held at V_{DD} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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ELECTRICAL CHARACTERISTICS

for 1000 Base-T Ethernet switching over recommended operating free-air temperature range, V_{DD} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]				MIN	TYP[2]	MAX	UNIT
V_{IK}	SEL, PD	V_{DD} = 3.6 V,	I_{IN} = −18 mA				−0.7	−1.2	V
I_{IH}	SEL, PD	V_{DD} = 3.6 V,	$V_{IN} = V_{DD}$					±2	μA
I_{IL}	SEL, PD	V_{DD} = 3.6 V,	V_{IN} = GND					±1	μA
I_{OFF}	SEL, PD	V_{DD} = 0 V,	V_{IN} = 0 to 3.6 V					±1	μA
I_{CC}		V_{DD} = 3.6 V,	$I_{I/O}$ = 0,	Switch ON or OFF			250	600	μA
I_{CC_PD}		V_{DD} = 3.6 V,	V_{IN} = 3.6 V,	PD = High			1		
C_{IN}	SEL, PD	f = 1 MHz,	V_{IN} = 0				2.6	3.0	pF
C_{OFF}	B or C port	V_I = 0,	f = 1 MHz,	Outputs open,	Switch OFF		3	4	pF
C_{ON}		V_I = 0,	f = 1 MHz,	Outputs open,	Switch ON		9	9.8	pF
r_{on}		V_{DD} = 3 V,	1.5 V ≤ V_I ≤ V_{DD},	I_O = −40 mA			4	8	Ω
$r_{on(flat)}$ [3]		V_{DD} = 3 V,	V_I = 1.5 V and V_{DD},	I_O = −40 mA			0.7		Ω
Δr_{on} [4]		V_{DD} = 3 V,	1.5 V ≤ V_I ≤ V_{DD},	I_O = −40 mA			0.8	1.5	Ω

(1) V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at V_{DD} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) $r_{on(flat)}$ is the difference of r_{on} in a given channel at specified voltages.
(4) Δr_{on} is the difference of r_{on} from center (A_4, A_5) ports to any other port.

ELECTRICAL CHARACTERISTICS

for 10/100 Base-T Ethernet switching over recommended operating free-air temperature range, V_{DD} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]				MIN	TYP[2]	MAX	UNIT
V_{IK}	SEL, PD	V_{DD} = 3.6 V,	I_{IN} = −18 mA				−0.7	−1.2	V
I_{IH}	SEL, PD	V_{DD} = 3.6 V,	$V_{IN} = V_{DD}$					±2	μA
I_{IL}	SEL, PD	V_{DD} = 3.6 V,	V_{IN} = GND					±1	μA
I_{OFF}	SEL, PD	V_{DD} = 0 V,	V_{IN} = 0 to 3.6 V					±1	μA
I_{CC}		V_{DD} = 3.6 V,	$I_{I/O}$ = 0,	Switch ON or OFF			250	600	μA
I_{CC_PD}		V_{DD} = 3.6 V,	V_{IN} = 3.6 V,	PD = High			1		
C_{IN}	SEL, PD	f = 1 MHz,	V_{IN} = 0				2.6	3.0	pF
C_{OFF}	B or C port	V_I = 0,	f = 10 MHz,	Outputs open,	Switch OFF		3	4	pF
C_{ON}		V_I = 0,	f = 10 MHz,	Outputs open,	Switch ON		9	9.8	pF
r_{on}		V_{DD} = 3 V,	1.25 V ≤ V_I ≤ V_{DD},	I_O = −10 mA to −30 mA			4	6	Ω
$r_{on(flat)}$ [3]		V_{DD} = 3 V,	V_I = 1.25 V and V_{DD},	I_O = −10 mA to −30 mA			0.5		Ω
Δr_{on} [4]		V_{DD} = 3 V,	1.25 V ≤ V_I ≤ V_{DD},	I_O = −10 mA to −30 mA			0.8	1.5	Ω

(1) V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at V_{DD} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) $r_{on(flat)}$ is the difference of r_{on} in a given channel at specified voltages.
(4) Δr_{on} is the difference of r_{on} from center (A_4, A_5) ports to any other port.

Product Folder Link(s): *TS3L501E*

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 3.3 V ± 0.3 V, R_L = 200 Ω, C_L = 10 pF
(unless otherwise noted) (see Figure 5 and Figure 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP[1]	MAX	UNIT
t_{pd} [2]	A or B/C	B/C or A		0.3		ns
t_{PZH}, t_{PZL}	SEL	A or B/C	0.5		15	ns
t_{PHZ}, t_{PLZ}	SEL	A or B/C	0.9		9	ns
$t_{sk(o)}$ [3]	A or B/C	B/C or A		50	100	ps
$t_{sk(p)}$ [4]	A or B/C	B/C or A		50	100	ps
t_{ON}/t_{OFF} [5]	PD	A or B/C			250	ns

(1) All typical values are at V_{DD} = 3.3 V (unless otherwise noted), T_A = 25°C.
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Output skew between center port (A_4 to A_5) to any other port
(4) Skew between opposite transitions of the same output in a given device $|t_{PHL} - t_{PLH}|$
(5) Device enable/disable time from PD

DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TYP[1]	UNIT
X_{TALK}	R_L = 50 Ω,	f = 250 MHz,	See Figure 8	–37	dB
O_{IRR}	R_L = 50 Ω,	f = 250 MHz,	See Figure 9	–37	dB
BW	See Figure 7			600	MHz

(1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

TS3L501E
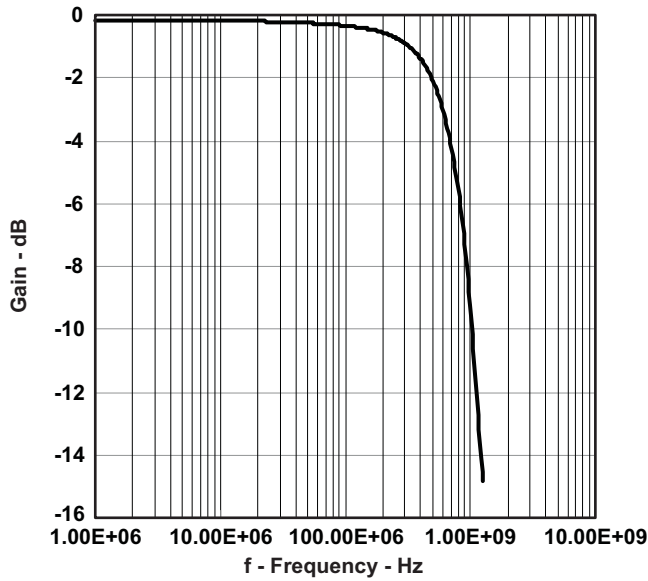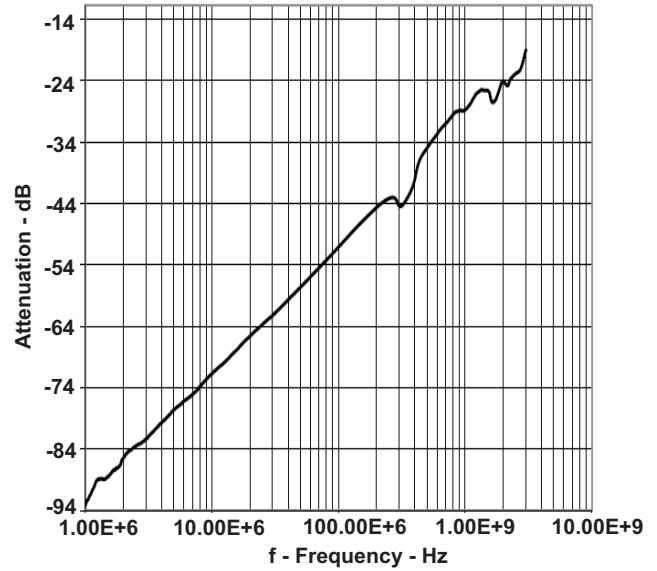
OPERATING CHARACTERISTICS

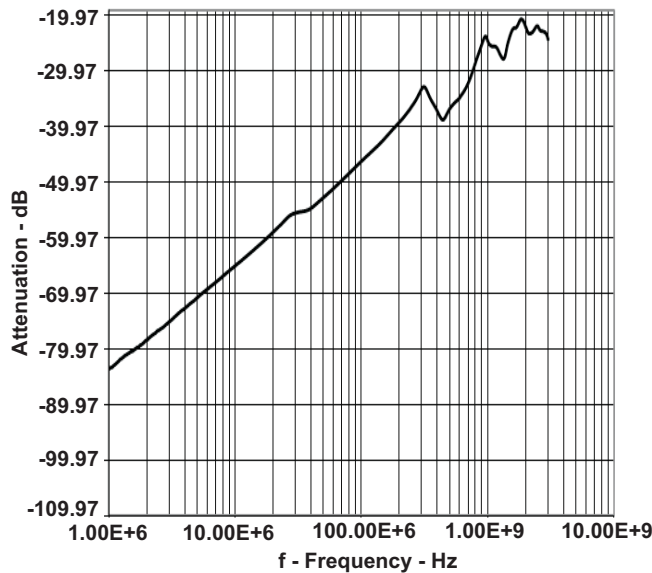Figure 1. Gain vs Frequency

Figure 2. OFF Isolation vs Frequency

Figure 3. Crosstalk vs Frequency

Figure 4. r_{on} (Ω) vs V_{com} (V)
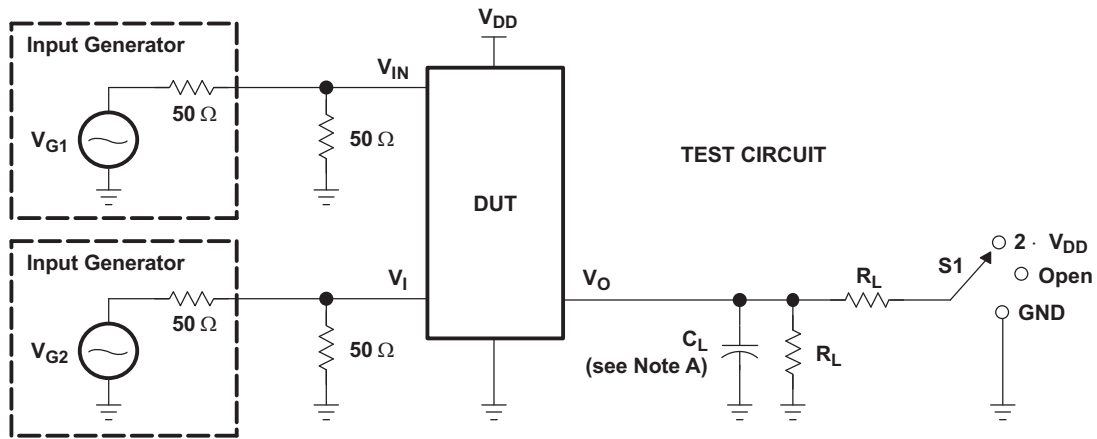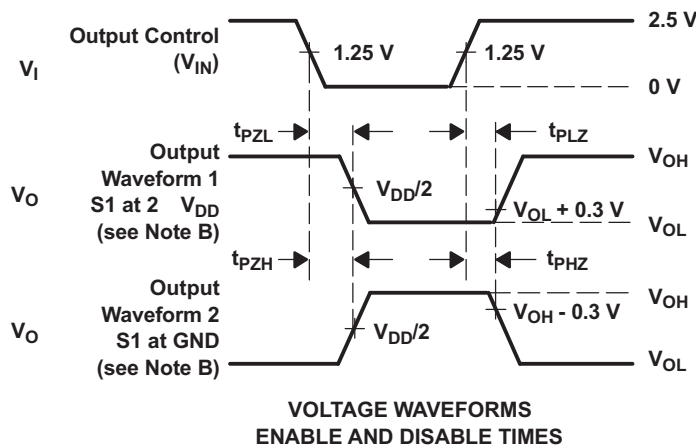
Product Folder Link(s): TS3L501E
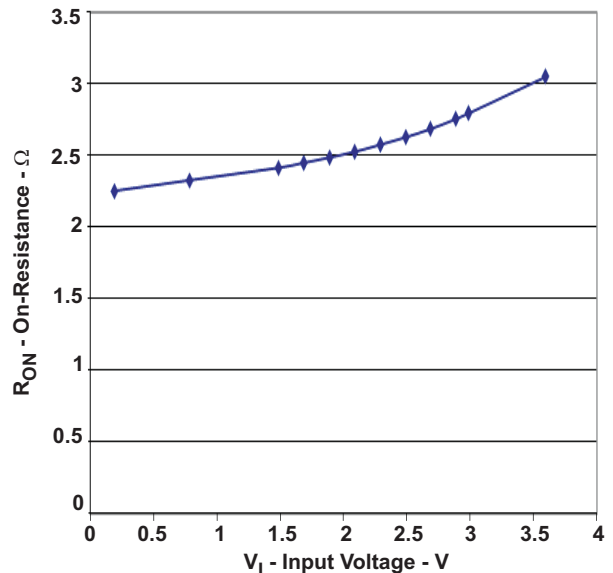
PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)

TEST	V_{DD}	S1	R_L	V_{in}	C_L	V_Δ
t_{PLZ}/t_{PZL}	3.3 V	2 · V_{DD}	200 Ω	GND	10 pF	0.3 V
t_{PHZ}/t_{PZH}	3.3 V	GND	200 Ω	V_{DD}	10 pF	0.3 V

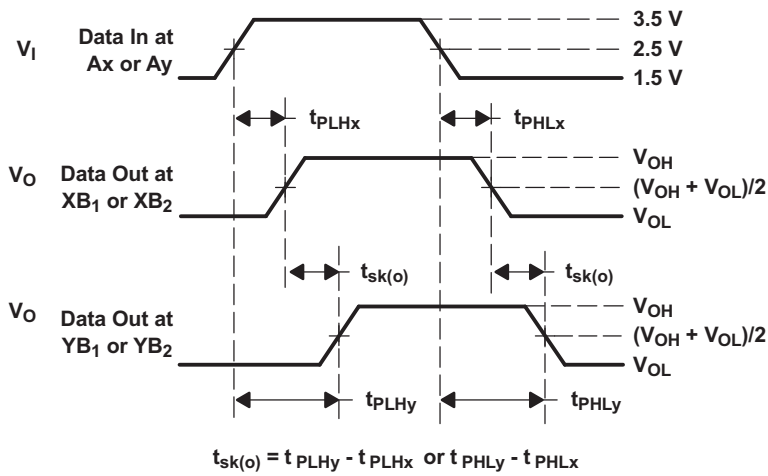**VOLTAGE WAVEFORMS**
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
          B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
              Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
          C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
          D. The outputs are measured one at a time, with one transition per measurement.
          E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
          F. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 5. Test Circuit and Voltage Waveforms

TS3L501E

PARAMETER MEASUREMENT INFORMATION
(Skew)
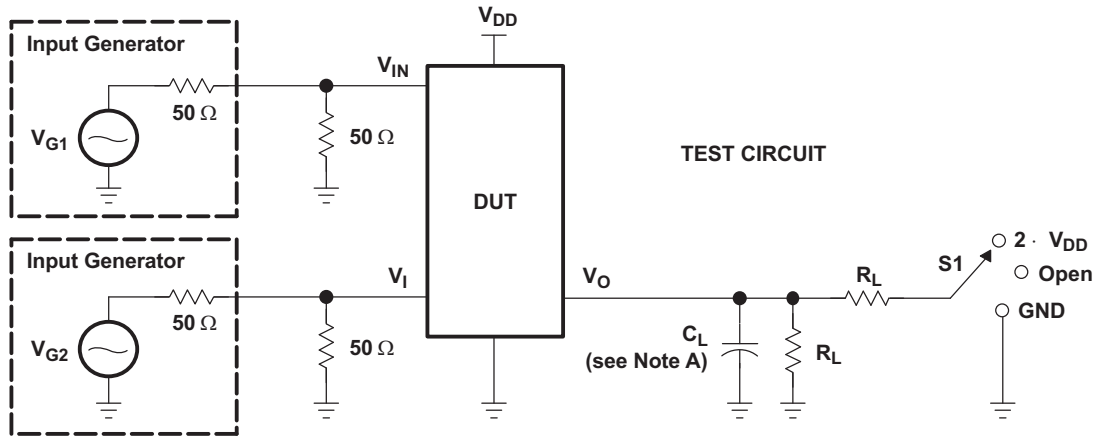
TEST	V_{DD}	S1	R_L	V_{in}	C_L
$t_{sk(o)}$	3.3 V ± 0.3 V	Open	200 Ω	V_{DD} or GND	10 pF
$t_{sk(p)}$	3.3 V ± 0.3 V	Open	200 Ω	V_{DD} or GND	10 pF

$$t_{sk(o)} = t_{PLHy} - t_{PLHx} \text{ or } t_{PHLy} - t_{PHLx}$$

VOLTAGE WAVEFORMS
OUTPUT SKEW ($t_{sk(o)}$)

$$t_{sk(p)} = t_{PHL} - t_{PLH}$$
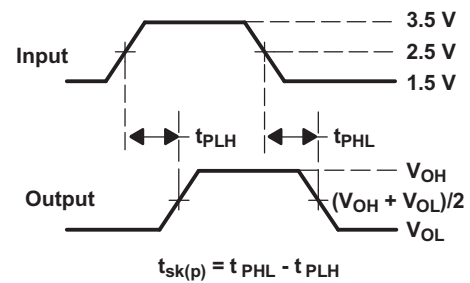
VOLTAGE WAVEFORMS
PULSE SKEW [$t_{sk(p)}$]

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, $Z_O = 50\,\Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 6. Test Circuit and Voltage Waveforms

Product Folder Link(s): *TS3L501E*

PARAMETER MEASUREMENT INFORMATION
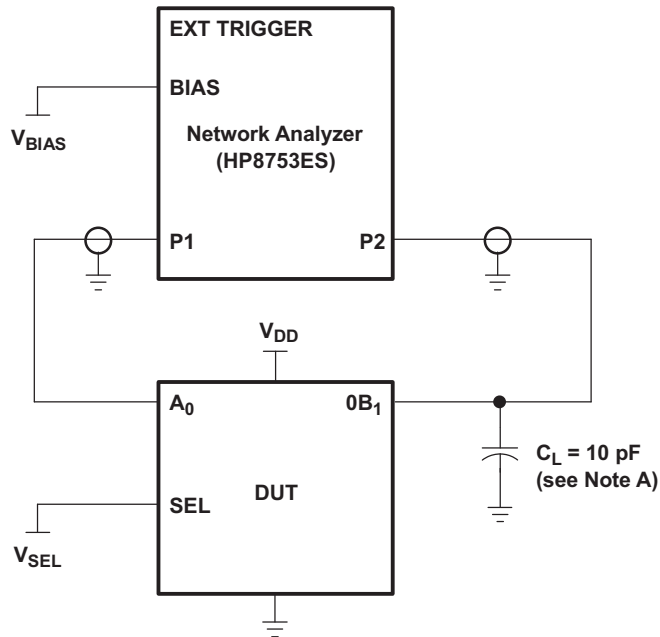
A. C_L includes probe and jig capacitance.
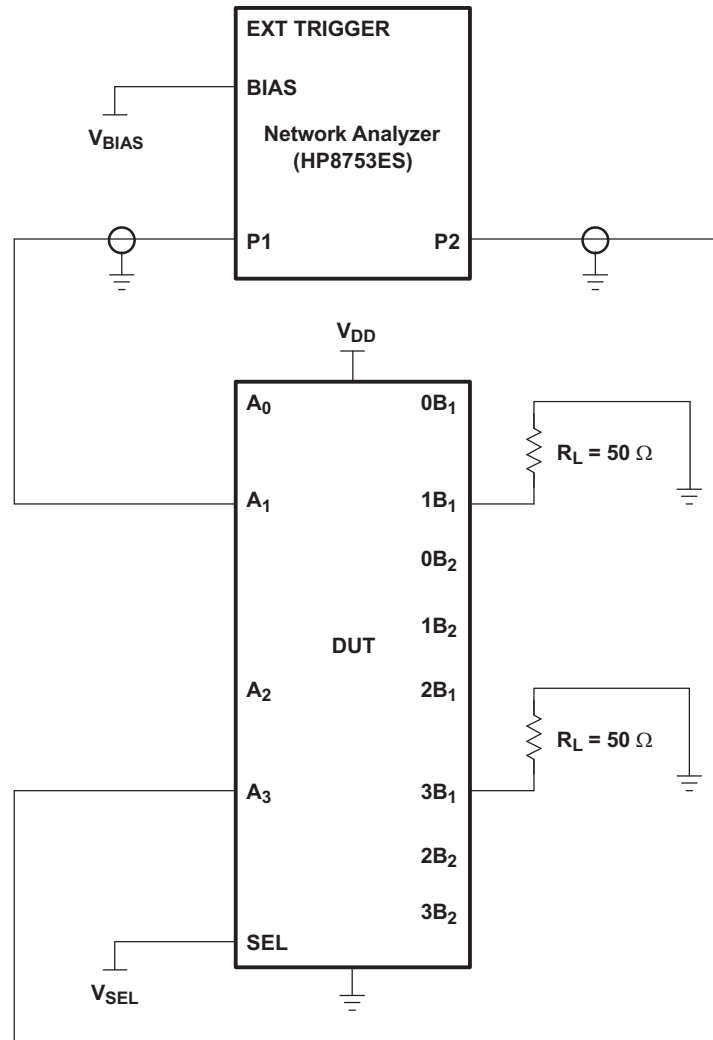
Figure 7. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_{SEL} = 0 and A_0 is the input, the output is measured at $0B_1$. All unused analog I/O ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

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PARAMETER MEASUREMENT INFORMATION (continued)

A. C_L includes probe and jig capacitance.

B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.
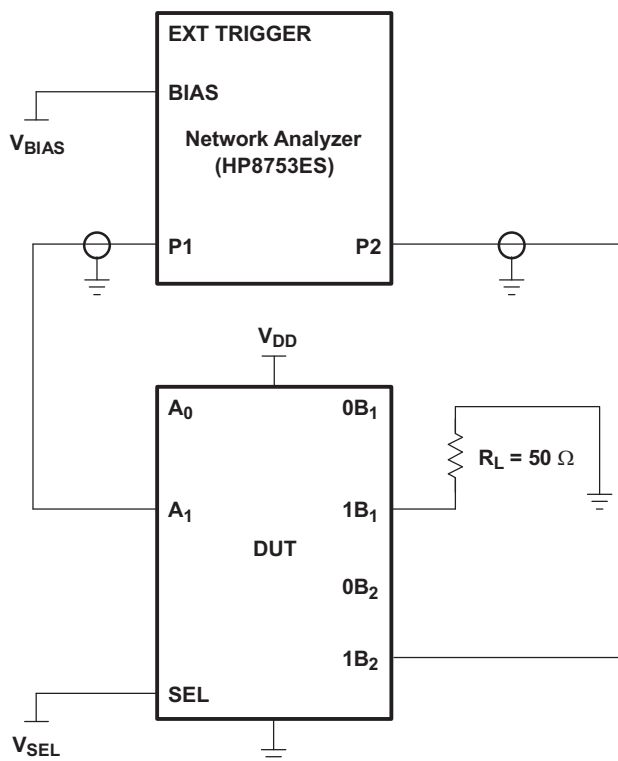
Figure 8. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when $V_{SEL} = 0$ and A_1 is the input, the output is measured at A_3. All unused analog input (A) ports are connected to GND, and output (B) ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)

A. C_L includes probe and jig capacitance.
B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.

Figure 9. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when V_{SEL} = GND and A_1 is the input, the output is measured at $1B_2$. All unused analog input (A) ports are connected to ground, and output (B) ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3L501ERUAR	ACTIVE	WQFN	RUA	42	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TK501E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
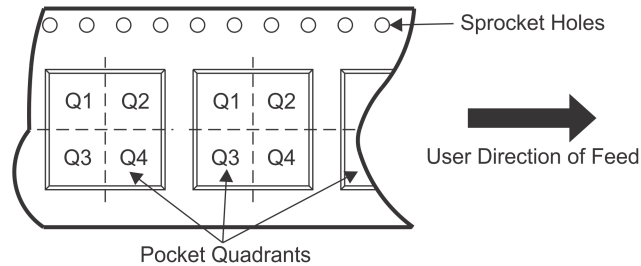
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3L501ERUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
TS3L501ERUAR	WQFN	RUA	42	3000	330.0	24.4	3.9	9.4	1.0	8.0	24.0	Q1
TS3L501ERUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3L501ERUAR	WQFN	RUA	42	3000	358.0	335.0	35.0
TS3L501ERUAR	WQFN	RUA	42	3000	346.0	346.0	35.0
TS3L501ERUAR	WQFN	RUA	42	3000	367.0	367.0	38.0

RUA (R−PWQFN−N42)　　　　　PLASTIC QUAD FLATPACK NO−LEAD

Pin 1 Index Area

0,20 Nominal
Lead Frame

Seating Plane

THERMAL PAD
SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

Bottom View

4208351/C 06/11
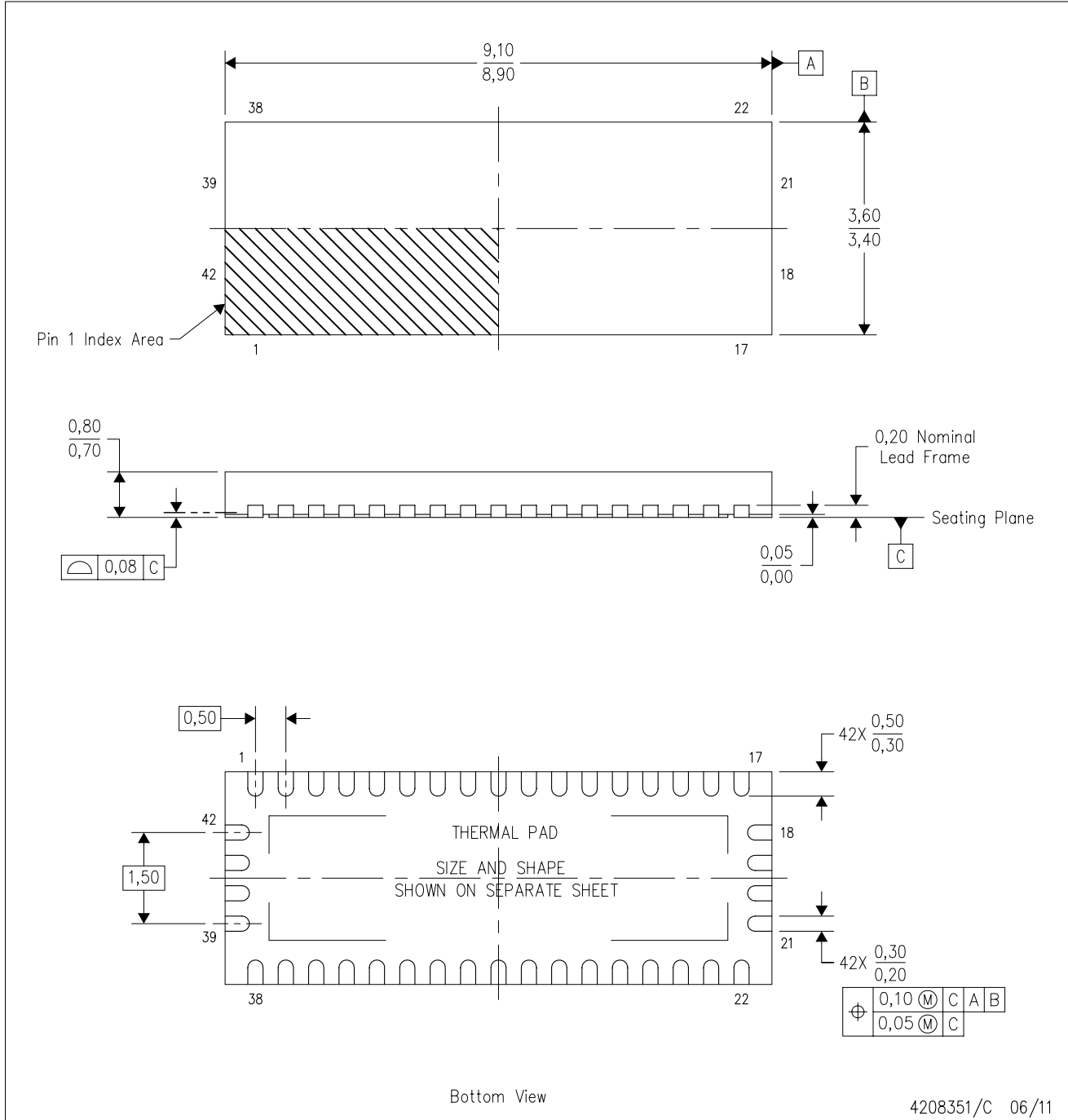
NOTES:　A.　All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　QFN (Quad Flatpack No−Lead) package configuration.
　　　　　D.　The package thermal pad must be soldered to the board for thermal and mechanical performance.
　　　　　E.　See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

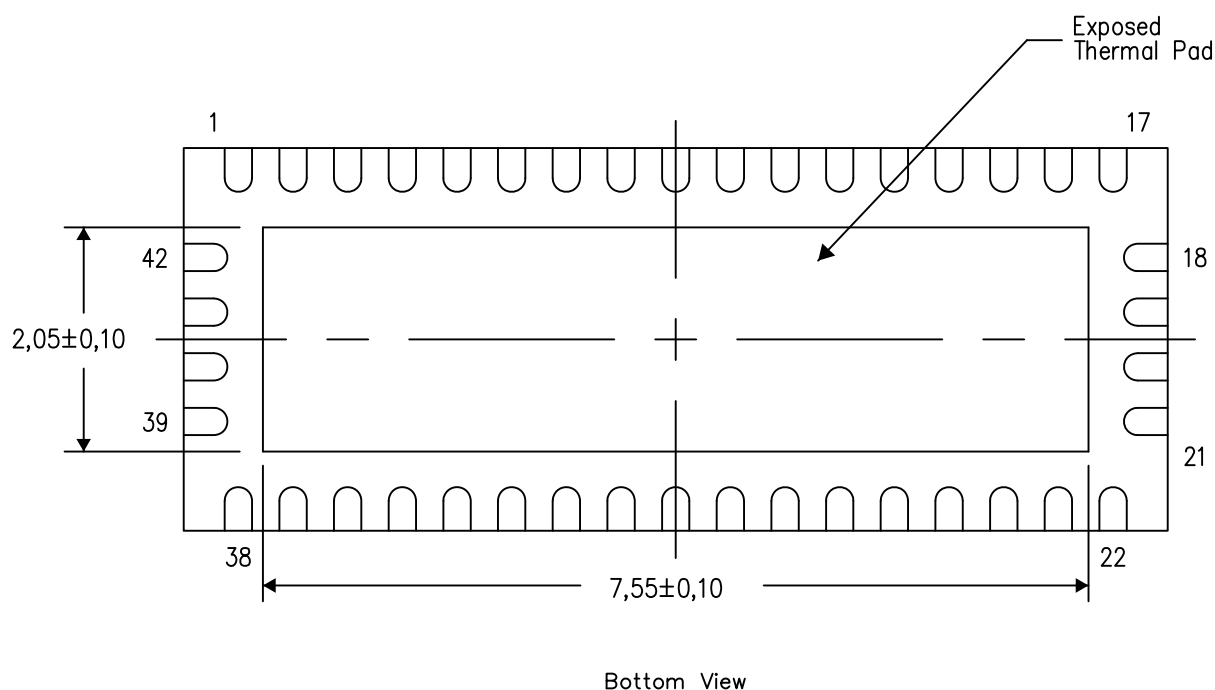RUA (R−PWQFN−N42)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
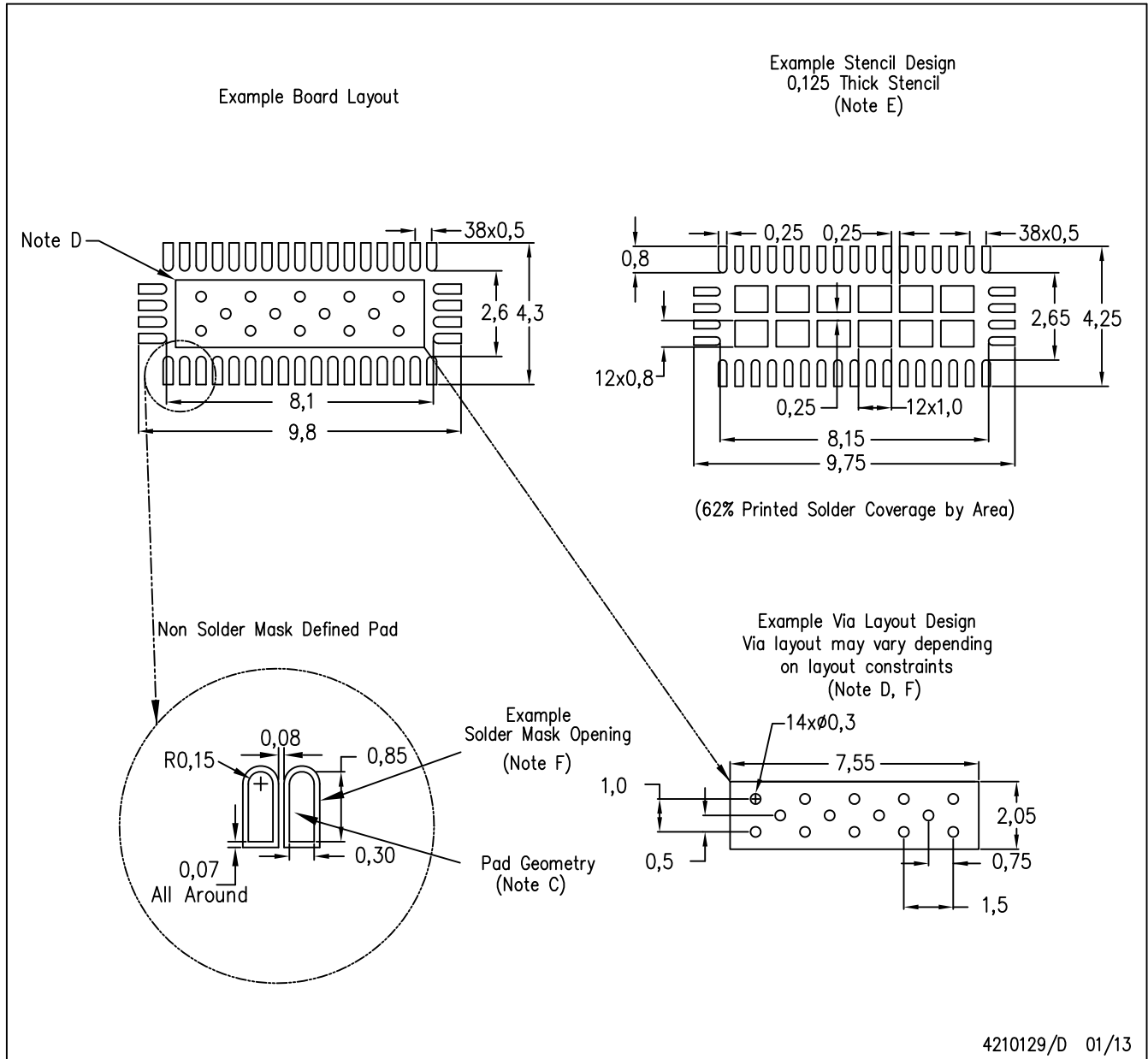

Bottom View

Exposed Thermal Pad Dimensions

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NOTE: All linear dimensions are in millimeters

RUA (R−PWQFN−N42)   PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

Example Stencil Design
0,125 Thick Stencil
(Note E)

Note D

38x0,5

2,6 4,3

8,1

9,8

0,8

0,25 0,25

38x0,5

2,65 4,25

12x0,8

0,25

12x1,0

8,15

9,75

(62% Printed Solder Coverage by Area)

Non Solder Mask Defined Pad

Example Via Layout Design
Via layout may vary depending
on layout constraints
(Note D, F)

14x⌀0,3

R0,15

0,08

0,85

0,07
All Around

0,30

Example
Solder Mask Opening
(Note F)

Pad Geometry
(Note C)

7,55

1,0

0,5

2,05

0,75

1,5

4210129/D   01/13

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate designs.
         D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack
             Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
             for specific thermal information, via requirements, and recommended board layout. These documents are available at
             www.ti.com <http: //www.ti.com>.
         E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
             recommendations for vias placed in the thermal pad.

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